Laboratory ADC Tester Based on NI-6251 Acquisition Card

M. Nikolić, M. Sokolović, and P. Petković

Abstract – Analog to digital converter (ADC) is the crucial part of many mixed-signal ICs because it interfaces analog signals from real world with digital logic on a chip. Faults made during ADC hardly can be repaired within the digital part. Therefore, functional testing of ADC is a very important task especially during prototyping. In this paper one laboratory ADC tester is proposed. It is based on NI-6251 data acquisition card and a PC that controls the testing process using LabView software.

I. INTRODUCTION

General purpose ADC testers are very expensive because of a wide variety of ADC architectures that require different testing techniques and equipment. Simultaneously, the testing process cannot improve the quality of individual ICs. It solely can measure the quality that already exists in an IC [1]. For a low volume production and for prototyping purposes it is not rational to spend a fortune for a professional tester. As an alternative, it is reasonable to develop a tester dedicated for the specific use.

In order to make testing possible, the designer has to provide testability of integrated circuit during design phase using various DFT methods [1]. Considering a prototype, it is significant not only to determine if circuit works or not but to detect how good it is and eventually how to fix potential faults in the subsequent design. Therefore, some signals that are not necessary for nominal operation of an IC, should be made observable for testing purposes by adding additional pins.

The major problems related to testing a prototype are controlling the test set-up conditions and observing the responses from a circuit under test (CUT).

Different blocks within a mixed signal microsystem, such as analog or digital signal processing parts, require different testing approaches. This makes ADC testing a difficult task.

Mutual interference of mixed signals is another issue that introduce troubles into the testing process. Namely, in highly integrated circuits, various sub-systems are in immediate proximity which causes influences to each other. Besides, the heat dissipated from a digital signal processor (DSP) affect operating points of analog circuitry.

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This paper describes ADC testing theory and realization of a laboratory tester based on NI-6251 data acquisition card [2]. The tester is dedicated for ADC implemented within an ASIC solid state energy meter named IMPEG, that was designed in our laboratory. The ADC was realized using sigma-delta architecture and the target characteristic was to obtain SFDR of at least 80dBc [2]. The tester can be modified and used for testing other ADCs with similar architectures and operating rates. DFT techniques implemented in IMPEG were described in [3]. The motive for the work described in this paper was to improve testing possibilities of the tester explained in [4] and to enhance measurement accuracy. The new tester utilizes the benefits of built-in DFT hardware.

This paper is organized in the following sections. The next section describes different ADC architectures. The third section deals with different methods for ADC testing. Some important variables to be measured during testing an ADC are listed here, as well. After that a practical implementation of one laboratory ADC tester will be given. This realization requires an original measurement and data processing procedure and is affordable to many non industrial users. The paper concludes with important results obtained after testing the particular sigma-delta ADC. These results verify the functionality of the entire test set-up.

II. ANALOG TO DIGITAL CONVERTERS

There are many different types of ADC architectures, that are introduced to fulfill the requirements of a specific application [1].

Successive approximation architectures provide DAC output adjusted with a binary search algorithm until it is substantially equal to the input voltage. This kind of ADCs is difficult to design and test and often suffer from nonidealities in approximation as well as poor linearity, hysteresis errors, poor power supply rejection ration and low bit rates [1, 5].

Integrating ADC (dual-slope and single-slope) is simpler but slower than the ADC architectures based on successive approximation. It uses a simple integrator to ramp upward for a fixed amount of time, starting from the time it crosses fixed threshold voltage [1, 5]. Dual-slope integrating ADCs have smaller offset errors, but are more complex than single-slope ADCs. They have better linearity.

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A flash ADC compare the input signal against all possible decision levels, simultaneously. This type of ADCs is very fast because the decision levels are compared all at once. They are mostly used in high-frequency application, but occupy much silicon area [1, 5]. Multiple flash ADCs can also be used to construct a multipass successive approximation architecture called a semiflash ADC [1].

Sigma-delta ADC uses a crude ADC combined with a noise-shaping process to produce an oversampled pulse density modulated (PDM) data stream. This data stream is then digitally filtered and decimated to produce high-resolution ADC samples [1, 5].

The use of oversampling sigma-delta modulators for high-resolution ADC resolves problems related to analog component limitations. Besides, it is able to meets all requirements for the specific design. Therefore this architecture was our choice.

Sigma-delta modulators employ coarse quantization enclosed in one or more feedback loops. By sampling at a frequency that is much greater than the signal bandwidth, it is possible for the feedback loops to shape the quantization noise so that most of the noise power is shifted out of the signal band. The out of band noise can then be attenuated with a digital filter. The degree to which the quantization noise can be attenuated depends on the order of the noise shaping and the oversampling ratio [2].

III. ADC TESTING

Typical tests capable to apprise quality of ADC are [1]:

- ADC code edge measurement,
- DC tests,
- transfer curve tests, and
- dynamic ADC tests.

Each one of them will be briefly explained.

The aim of ADC code edge measurement is to find the input voltage threshold between two successive ADC codes that causes an output code to change. To measure the ADC linearity one needs to derive transfer curve of an ADC. Two well-known methods for transfer curve derivation are center code testing and edge code testing [1].

Code centers are defined as the midpoint between the code edges. This is shown in Figure 2. The most obvious method to find the edge is a step search method where one simply adjusts the input voltage of the ADC up or down until the output codes are evenly divided between the first code and the second code. To achieve repeatable results, one needs to collect about 50 to 100 samples from the ADC in order to provide statistically significant number of conversions.

Another edge search technique is a servo method. This is a fast hardware version of the step search. Using this hardware, the output codes from ADC are compared against a value programmed in the search value register. If the ADC output is greater than or equal to the expected value, the integrator ramps downward. On the contrary, the integrator ramps upward.

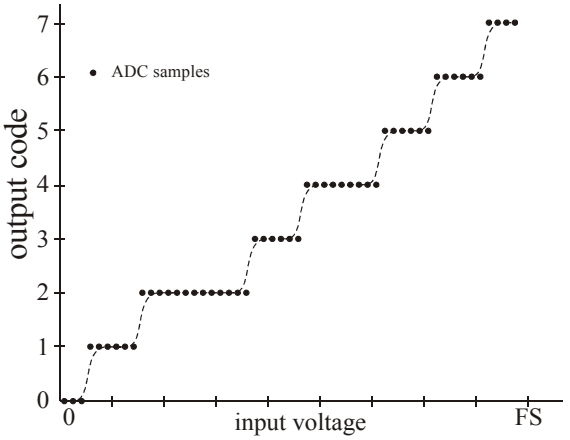

Fig. 2. ADC samples from linear ramp histogram test

But the most common production testing technique is the histogram method. The simplest way to perform a histogram test is to apply a rising or falling linear ramp to the input of the ADC and collect samples from the ADC at constant sampling rate. The ADC samples are captured while the input ramp slowly moves from one end of the ADC conversion range to the other. This is shown in Figure 3. The number of occurrences of each code is plotted as a histogram. It shows which codes are hit more often, indicating that they are wider codes. After obtaining the histogram, a code edge transfer curve must be derived using a simple mathematical equation that sums the code widths.

To compensate for the poor linearity of the ramp generators, the alternative: sinusoidal histogram method can be performed. It is easier to produce a pure sinusoidal waveform than to produce a perfectly linear ramp. This method also allows testing in more dynamic, real-world situation, since ramps are varying very slowly. By using a sinusoidal signal instead of a ramp, one would expect to get more code hits at the upper and lower codes than at the center of the ADC transfer curve, even when testing a perfect ADC. The effects of the nonuniform voltage distribution can be removed after normalization.

DC Tests and Transfer Curve Tests comprise:

- DC Gain,
- DC offset,
- Integral nonlinearity, INL,
- Differential nonlinearity, DNL,
- monotonicity and
- missing codes tests.

Once the ideal transfer curve has been established, DC gain and offset can be measured. The gain and offset are measured by calculating the slope and offset of the best-fit line. ADC can be nonmonotonic when one or more of its code widths is negative. However, this failure mechanism is quite rare. Nevertheless, ADC can appear to be nonmonotonic when its input is changing rapidly. ADCs are not tested for monotonicity with a slowly changing input.

Monotonicity errors show up as signal-to-noise ratio failures and as a sparkling.

The code whose voltage width is zero is recognized as a missing code. This means that the missing code can never be hit, regardless of the ADC's input voltage. A missing code appears as a missing step on an ADC transfer curve.

Dynamic ADC parameters are: maximum sampling frequency, maximum conversion time, and minimum recovery time. Maximum conversion time is the maximum amount of time it takes an ADC to produce a digital output after a stabile input signal is asserted. The ADC is guaranteed to produce a valid output within the maximum conversion time.

Considering all tests listed and an existing ADC architecture, it is very important to determine the significance and the feasibility of tests to be performed. Tests such as INL and DNL are not well suited for sigma-delta converters. Instead, channel tests like gain, offset, signal-to-noise ratio, idle channel noise, etc., are commonly specified. When the resolution exceeds 12 or 13 bits, it becomes very expensive to perform transfer curve test such as INL and DNL because of the large number of code edges that must be measured. Fortunately, transmission parameters such as frequency response signal to distortion ratio and idle channel tests are much less time-consuming to measure [1]. A limited budget also limits the list of tests that can be performed in the laboratory environment. For example, dual-slope integrating ADCs have good linearity. For this type of architectures, all-codes testing would be prohibitively expensive for production testing.

One of the best ways to overcome different testing problems is to apply the concept of DSP-based testing [1]. It is based on special digital signal processing tools that could be implemented on the CUT, that is hardware, or written as particular software. This offers several advantages over the traditional measurement techniques. One can create and measure signals with multiple frequencies at the same time, and in that way, one can perform many parametric measurements in parallel. Thus, the test time is reduced. Separation of different signal components gives a second huge advantage over non-DSP-based measurements. We can isolate noise and distortion components from one another and from the test tones, which allows much more accurate and repeatable measurements. The third big advantage of this method is the ability for signal manipulation. Just one set of output signal samples allows the manipulation of the waveforms to achieve a variety of results.

IV. TEST SET-UP

Analog part of IMPEG consists of two sigma-delta A/D converters. Second order sigma-delta modulator is in voltage channel, while third order sigma-delta modulator is in current channel. Sampling frequency is 524288 Hz and required data rate for built-in DSP is 4,096kHz. In order to make converted digital signals observable, three pins were added for testing purposes before decimation. One stands for output from the voltage and two for the output from the current channel. ADC in current channel is implemented using MASH architecture [6, 7] and hence, the output is composed of two single-bit signals. The voltage channel should result with dynamic range, SNR and SFDR greater then 60dB. Stringent requirements are imposed for current channel, with dynamic range, SNR and SFDR greater then 80 dB.

Therefore the resolution of stimulus generator must be greater then 14 bits to satisfy imposed requirements. Acquired data are processed further by FFT. The acquisition time has to last at least two seconds in real time to provide enough data to perform FFT. After FFT analysis one can obtained values of SNDR, SFDR and linearity of ADC. Besides, the collected input data have to provide information necessary for fault detection and diagnostics.

Figure 4 shows the proposed tester set-up. It consists of :

- an original printed circuit board containing circuit under test,
- NI-6251 data acquisition card and
- PC that controls the testing process using LabView software.

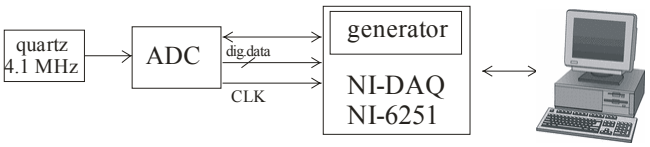

Fig. 4. ADC test set-up

DAQ card offers:

- 16 (8 differential) analog inputs each with 16 bit resolution and maximum sampling frequency of 1.25 Msamples/s,
- three 8 bit digital ports where only one can be hardware timed up to 10 MHz and
- two analog outputs with 2.8Msamples/s at most and can generate arbitrary shaped waveform.

Stimulus is sinewave generated as differential signal occupying both analog output channels of DAQ card. Simultaneously, the card utilizes two channels to acquire analog input data in order to check signal integrity. The collected data represent signal obtained after analog LP filter with cut-off frequency of 2kHz according to Figure 5.

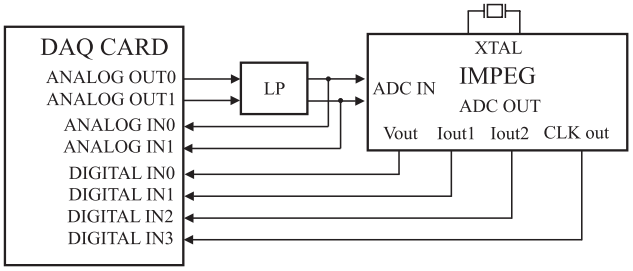

Fig. 5. Block diagram of interconnection between acquisition card and IMPEG

Three digital input channels are used to acquire digital output from voltage and current channel. An additional digital input serves to control digital acquisition by the clock signal generated in IMPEG.

This setup can be used for testing different kinds of ADC's, such as: sigma-delta as shown here, successive approximation architecture, flash etc.

The testing possibilities restrict the number of available digital lines and sampling frequency. Besides, limitation arise from maximal input signal frequency and/or digital signal resolution.

V. Measurement and Results

Figure 6 shows test results obtained for the ADC implemented within the voltage channel of IMPEG. The power spectrum obtained after stimulus with amplitude of 40mVpp differential sinewave signal and frequency of 50Hz, applied to ADC input is shown in Figure 6.a. Figure 6.b presents the power spectrum of output signal acquired with the second order sigma-delta ADC. In order to verify design methodology the same input signal is used as stimuli for behavioral simulation of the sigma-delta modulator in voltage channel. Figure 6.c illustrates the corresponding power spectrum. Obviously, very good matching with behavioral model and measurement was obtained.

VI. Conclusion

Tester realization required development of specific hardware and software solutions. All tests performed in the laboratory setting were proved in real environment within the energy meter device developed by our industrial partner. The implemented testing method is very simple and offers low cost functional oriented testing that gives a good base for diagnostics as well.

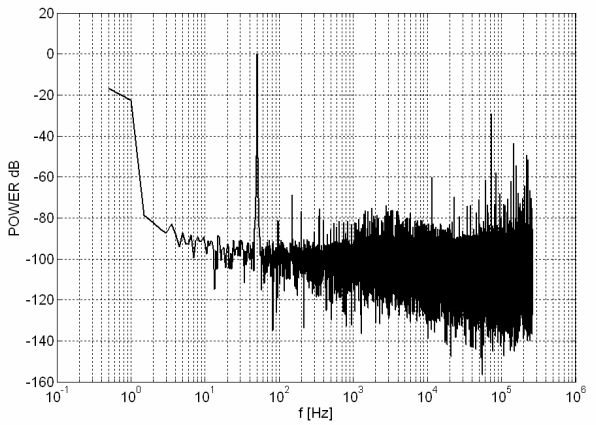

Fig. 6. a) Power spectrum of input signal; Hanning window

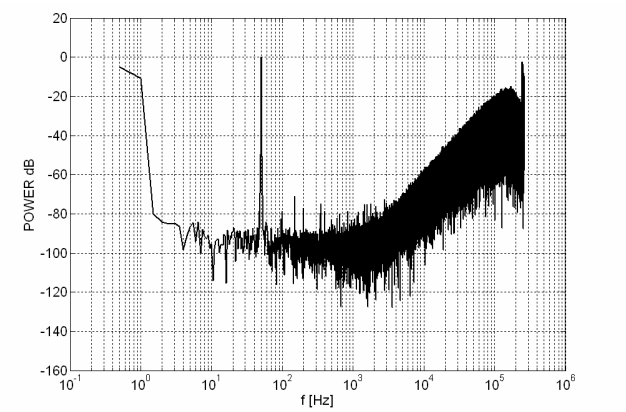

Fig 6. b) spectrum of the ADC output signal; Hanning window

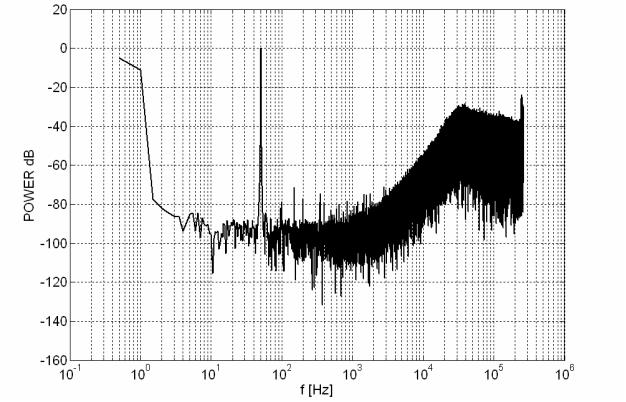

Fig. 6. c) spectrum of the ADC ouput signal behavioral level; Hanning window

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